Core Topics

1. Fundamentals Of Digital Design
2. VHDL
3. VERILOG
4. SYSTEM VERILOG
5. 2 Major Project

FUNDAMENTALS OF DIGITAL DESIGN

Introduction to VLSI
- What is VLSI
- VLSI Design Flow
- ASIC
- SoC

Fundamentals
- Basic Digital Circuits
- Logic gates & Boolean Algebra
- Number Systems
- Digital Logic Families

Combinational Logic Design
- Multiplexers
- MUX based design for digital circuits
- Demultiplexers/Decoders
- Adders/Subtractors
- BCD Arithmetic & ALU
- Comparators & Parity Generator
- Code Converters/Encoders
- Decoders
- Multipliers/Divider

Sequential Logic Design Principles
- Bistable Elements.
- Latches and Flip-Flops
Counters and its application
Synchronous Design Methodology
Impediments to Synchronous Design
Shift Registers
Design Examples & Case studies

Advanced Digital Design
- Synchronous/Asynchronous Sequential Circuits
- Clocked Synchronous State-Machine Analysis
- Clocked Synchronous State-Machine Design
- Finite state machine
- Mealy and Moore machines
- State reduction technique
- Sequence Detectors
- ASM Charts
- Synchronizer Failure and Metastability Estimation
- Clock Dividers
- Synchronizers & Arbiters
- FIFO & Pipelining
- PLD + CPLD

VHDL
- VHDL OVERVIEW AND CONCEPTS: Types, object classes, design units, compilation, elaboration.
- BASIC LANGUAGE ELEMENTS: Lexical elements, syntax, operators, types and subtypes (scalar, physical, real, composite (arrays, records), access, file).
- CONTROL STRUCTURES: Control structures and rules (if, case, loop).
- DRIVERS: Resolution function, drivers (definition, Initialization, creation, ports)
- TIMING: Signal attributes, "wall" statement, delta time, simulation engine, modeling with delta time delays, VITAL tables, Inertial / transport delay
- ELEMENTS OF ENTITY/ARCHITECTURE: Entity, architecture, (process, concurrent signal assignment, component instantiation and port association rules, concurrent procedure, generates concurrent assertion, block, guarded signal).
- SUBPROGRAMS: Rules and guidelines (unconstrained arrays, interface class, initialization, implicit signal attributes, drivers, signal characteristics in procedure calls, side effects), overloading, functions (resolution function, operator overloading), concurrent procedure.
- PACKAGES: Declaration, body, deferred Constant, 'use' Clause, Signals, resolution function, subprograms, converting typed objects to strings, TEXTIO, printing objects, linear feedback shift register, random number generation compilation order
- USER DEFINED ATTRIBUTES, SPECIFICATIONS, AND CONFIGURATIONS: Attribute declarations, attributes specifications, configuration specification and binding, configuration declaration and binding, configuration of generate statements.
- **DESIGN FOR SYNTHESIS:** Constructs, register inference, combinational logic inference, state machine and design styles, arithmetic operations.
- **FUNCTIONAL MODELS AND TESTBENCHES:** Test bench design methodology, BFM Modeling, scenario generation schemes, waveform generator, client/server, text command file, binary command file.
- **MINOR PROJECT**
- **VITAL:** Overview, features, model, pin-to-pin delay modeling style, distributed delay modeling style.
- **Lab Sessions on ModelSIM**

**VERILOG**

- **Overview of Digital Design with Verilog HDL**
  Evolution of CAD, emergence of HDLs, typical HDL-based design flow, why Veiling HDL?, trends in HDLs.
- **Hierarchical Modeling Concepts**
  Top-down and bottom-up design methodology, differences between modules arid module Instances, parts of a simulation, design block, stimulus block.
- **Basic Concepts**
  Lexical conventions, data types, system tasks, compiler directives.
- **Modules and Ports**
  Module definition, port declaration, connecting ports, hierarchical name referencing.
- **Gate-Level Modeling**
  Modeling using basic Verilog gate primitives, description of and/or arid buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
- **Dataflow Modeling**
  Continuous assignments, delay specification, expressions, operators, operands, operator types.
- **Behavioral Modeling**
  Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.
- **Tasks and Functions**
  Differences between tasks and functions, declaration, Invocation, automatic tasks and functions.
- **Useful Modeling Techniques**
  Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

**Advanced Verilog Topics**

- **Timing and Delays**
  Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.
- **Switch-Level Modeling**
  MOS and CMOS switches, bidirectional switches, modeling of power and ground, resistive switches, delay specification on switches.

- **User-Defined Primitives**
  Parts of UDP, UDP rules, combinational UDPs, sequential UDPs, shorthand symbols.

- **Logic Synthesis with Vernog HDL**
  Introduction to logic synthesis, impact of logic synthesis, Verilog HDL constructs and operators for logic synthesis, synthesis design flow, verification of synthesized circuits, modeling tips, design partitioning.

- **Advanced Verification Techniques**
  Introduction to a simple verification flow, architectural modeling, test vector/testbenches, simulation acceleration, emulation, analysis/coverage, assertion checking, formal verification, semi-formal verification, equivalence checking.

- **RTL Coding Style**

**LEVEL 2**

**Introduction to ASIC DESIGN METHODOLOGY**
- Typical Design Flow
- Specification and RTL Coding
- Dynamic Simulation
- Constraints, Synthesis
- Formal Verification
- Static Timing Analysis
- Placement Routing and Verification
- Engineering Change Order

**Front End Implementation**

**SYNTHESIS**
- Synthesis Environment
- Design Constraint
- Design Entry
- Technology Library
- Delay Calculation
- Delay Model

**PARTITIONING AND CODING STYLES**
- Partitioning for Synthesis
- RTL: Software Vs Hardware
- General guidelines
  - Technology Independence
  - Clock Logic
  - Clock Stretching
  - Guidelines for FSM synthesis
- Logic Inference
  - Memory element inference
  - Multiplexer Inference
  - Three state inference
SYSTEM VERILOG

Data types:
- Integer data type
- Real and short real
- Void data types
- Strings
- Event
- User defined
- Data declaration- Constant variables net reg logic signal aliasing
- Enumerations
- Structure and union
- Classes
- Casting

Arrays
- Packed and unpacked
- Dynamic arrays
- Queues

Operators and Expressions
- Arithmetic
- Logical
- Operator loading
- Conditional

Procedural statements and Control flow
- Blocking and non blocking assignments
- Selection statements
- Loops
- Jump
- Final block
- Named block
- Event control
- Level sensitive seq. control

Task and functions
- Argument passing
- Import and export functions

Classes
- Intro
- Object and its properties and methods
- Constructor
- Inheritances
- Sub classes
- Overridden members
- Super class
- Casting
- Data hiding and encapsulation
- Constant class and virtual methods
- Polymorphism

Assertions
- Immediate assertion
- Concurrent assertion overview
- Boolean exp
- Seq.
- Sequence operation
- Manipulating data in sequence
- Calling sub routines on the match of sequence
- Concurrent assertions

LIST OF PROJECTS
- Microcontroller Design
- RISC & CISC Processor Design
- Multiplier /Divider using different Algorithms
- DDR Controller
- I2C, AMBA, Wishbone Conmax
- JTAG: Boundary SCAN
- JPC, PCI, Ethernet
- CORD IC Algorithm

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